6.3 Register Maps

The devices contain three peripheral register spaces. The spaces are categorized as follows:

Peripheral Frame 0: These are peripherals that are mapped directly to the CPU memory bus. See Table 6-8.

Peripheral Frame 1: These are peripherals that are mapped to the 32-bit peripheral bus. See Table 6-9.

Peripheral Frame 2: These are peripherals that are mapped to the 16-bit peripheral bus. See Table 6-10.

Table 6-8. Peripheral Frame 0 Registers(1)

NAME	ADDRESS RANGE	SIZE (×16)	EALLOW PROTECTED(2)
Device Emulation Registers	0x00 0880 – 0x00 0984	261	Yes
System Power Control Registers	0x00 0985 – 0x00 0987	3	Yes
FLASH Registers(3)	0x00 0A80 – 0x00 0ADF	96	Yes
Code Security Module Registers	0x00 0AE0 – 0x00 0AEF	16	Yes
ADC registers (0 wait read only)	0x00 0B00 – 0x00 0B0F	16	No
CPU–TIMER0/1/2 Registers	0x00 0C00 – 0x00 0C3F	64	No
PIE Registers	0x00 0CE0 – 0x00 0CFF	32	No
PIE Vector Table	0x00 0D00 – 0x00 0DFF	256	No

(1) Registers in Frame 0 support 16-bit and 32-bit accesses.
(2) If registers are EALLOW protected, then writes cannot be performed until the EALLOW instruction is executed. The EDIS instruction disables writes to prevent stray code or pointers from corrupting register contents.
(3) The Flash Registers are also protected by the Code Security Module (CSM).

Table 6-9. Peripheral Frame 1 Registers

NAME	ADDRESS RANGE	SIZE (×16)	EALLOW PROTECTED
Comparator 1 registers	0x00 6400 – 0x00 641F	32	(1)
Comparator 2 registers	0x00 6420 – 0x00 643F	32	(1)
ePWM1 + HRPWM1 registers	0x00 6800 – 0x00 683F	64	(1)
ePWM2 + HRPWM2 registers	0x00 6840 – 0x00 687F	64	(1)
ePWM3 + HRPWM3 registers	0x00 6880 – 0x00 68BF	64	(1)
ePWM4 + HRPWM4 registers	0x00 68C0 – 0x00 68FF	64	(1)
eCAP1 registers	0x00 6A00 – 0x00 6A1F	32	No
GPIO registers	0x00 6F80 – 0x00 6FFF	128	(1)

(1) Some registers are EALLOW protected. See the module reference guide for more information.

Table 6-10. Peripheral Frame 2 Registers

NAME	ADDRESS RANGE	SIZE (×16)	EALLOW PROTECTED
System Control Registers	0x00 7010 – 0x00 702F	32	Yes
SPI-A Registers	0x00 7040 – 0x00 704F	16	No
SCI-A Registers	0x00 7050 – 0x00 705F	16	No
NMI Watchdog Interrupt Registers	0x00 7060 – 0x00 706F	16	Yes
External Interrupt Registers	0x00 7070 – 0x00 707F	16	Yes
ADC Registers	0x00 7100 – 0x00 717F	128	(1)
I2C-A Registers	0x00 7900 – 0x00 793F	64	(1)

(1) Some registers are EALLOW protected. See the module reference guide for more information.

6.4 Device Emulation Registers

These registers are used to control the protection mode of the C28x CPU and to monitor some critical device signals. The registers are defined in Table 6-11 .

Table 6-11. Device Emulation Registers

NAME	ADDRESS RANGE	SIZE (x16)	DESCRIPTION			EALLOW PROTECTED
DEVICECNF	0x0880 0x0881	2	Device Configuration Register			Yes
PARTID	0x3D 7FFF	1	Part ID Register	TMS320F280200PT	0x00C1	No
				TMS320F280200DA	0x00C0	
				TMS320F28027PT	0x00CF	
				TMS320F28027DA	0x00CE	
				TMS320F28027**F**PT	0x00CF	
				TMS320F28027**F**DA	0x00CE	
				TMS320F28026PT	0x00C7	
				TMS320F28026DA	0x00C6	
				TMS320F28026**F**PT	0x00C7	
				TMS320F28026**F**DA	0x00C6	
				TMS320F28023PT	0x00CD	
				TMS320F28023DA	0x00CC	
				TMS320F28022PT	0x00C5	
				TMS320F28022DA	0x00C4	
				TMS320F28021PT	0x00CB	
				TMS320F28021DA	0x00CA	
				TMS320F28020PT	0x00C3	
				TMS320F28020DA	0x00C2	
CLASSID	0x0882	1	Class ID Register	TMS320F280200PT/DA	0x00C7	No
				TMS320F28027PT/DA	0x00CF	
				TMS320F28027**F**PT/DA	0x00CF	
				TMS320F28026PT/DA	0x00C7	
				TMS320F28026**F**PT/DA	0x00C7	
				TMS320F28023PT/DA	0x00CF	
				TMS320F28022PT/DA	0x00C7	
				TMS320F28021PT/DA	0x00CF	
				TMS320F28020PT/DA	0x00C7	
REVID	0x0883	1	Revision ID Register	0x0000 - Silicon Rev. 0 - TMS		No
				0x0001 - Silicon Rev. A - TMS		
				0x0002 - Silicon Rev. B - TMS		